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Design Of 8BIT ALU using Tanner Tool V12.5

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Abstract—*In this paper implementation of 8-bit arithmetic logic unit (ALU) is presented. The design was implemented using SPICE code and Tanner tool V12.5.A 8-bit ALU (Arithmetic Logic Unit) has been designed for 3V operation. ALU (Arithmetic logic unit) is a critical component of a microprocessor and the core component of central processing unit. [1] Furthermore, it is the heart of the instruction execution portion of every computer. ALU's comprise the combinational logic that implements logic operations, such as AND, OR, EXOR and NOT and arithmetic operations, such as ADD and SUBTRACT.An arithmetic logic unit (ALU) is a digital circuit which performs arithmetic, logic and shift operations on two n-bit digital words.*

Keywords*: ALU, CMOS, logicgate, Tanner Tool V12.5, level 49 at 0.5 microtechnologies SPICE.*

1. INTRODUCTION

Functionally, an ALU can be divided up into three circuits: the arithmetic circuit, the logic circuit and the shift circuit.

i)The arithmetic circuit performs typical arithmetic operations such as addition, subtraction and increment or decrement by one. The basic component of an arithmetic circuit is the Full adder. By using a multiplexer to control the data inputs to the adder, it is possible to obtain different types of arithmetic operations.[2]Depending on the selection inputs and the input carry, the arithmetic circuit can generates the different arithmetic micro operations listed **Table 1**

Table 1: Function table of the arithmetic Circuit

S1	S0	Cin	Input	Output	Micro operation
0	0	0	B	A+B	Add
0	0	1	B	A+B+1	Add with cry
0	1	0	B'	A+B'	Sub with borrow
0	1	1	B'	A-B	Sub
1	0	0	0	A	Transfer A
1	0	1	0	A+1	Increment by 1
1	1	0	1	A-1	Decrement A by1
1	1	1	1	A	Transfer A

ii) The ALU, logic circuit performs the basic logic micro operations: NOT, AND, OR and XOR. From these four micro operations all known logic micro operations canbe derived. Figure 1-10 shows the logic diagram for one stage of logic circuit. The four gates generate the four logic operations and the multiplexer select the desiredoperation as shown in **Table 2.**

Table 2: Function table of the 2-bit Logic Circuit

S1	S0	Output	Operation
0	0	AB	AND
0	1	A+B	OR
1	0	A⊕B	XOR
1	1	A'	Complement

iii) Shift circuit used to perform the shift micro operations. The contents of a register can be shifted serially to the left or to the right. The shift circuit contains multiplexers as shown in Figure 5-3. when the select line is 0 the 4-bit input data are shifted right. When the select line is 1 the input data are shifted left. There are two serial inputs one for shift left and other one for shift right. The function table shows the outputs of the multiplexers in each case. **Table 3.**

Table 3: Function table of the 4-bit Shift Circuit

S	H3			
	H3	H2	H1	H0
0	IR	A3	A2	A1
1	A2	A1	A0	IL

Block Diagram for Designing of ALU

ALU design by following the correct procedure some introductory part is given as**,** Making the programming,draw the schematic diagram, and for the layout diagram at each and every step check the DRC for the proper designing [2]. The design of the 8-bit ALU is based on the use of a carry select line, implemented using AMI's C5N process. Once verification was completed parasitic were extracted. To create a test for finding the maximum operating frequency a pseudo-random input stream was applied to each input of the ALU and observed the circuit during the input transition. If the switching of the transistors takes longer than the period of the input then the ALU may give a erroneous output. **Figure shown below**shows the step by step procedure for the ALU designing

2. CIRCUIT DESIGN

There are different circuit use for the designing of the ALU, schematic and waveform (DC and AC Analysis) some of them are as follows:

A) Inverter

An inverter or NOT gate is logic gate which an inverter circuit outputs a voltage representing the opposite logic-level to its input. Inverters can be constructed using a single NMOS transistor or a single PMOS transistor coupled with a resistor. Since this 'resistive-drain' approach uses only a single type of transistor, it can be fabricated at low cost. However, because current flows through the resistor in one of the two states, the resistive-drain configuration is disadvantaged for power consumption and processing speed implements logical negative.

The truth table is shown in table

Schematic

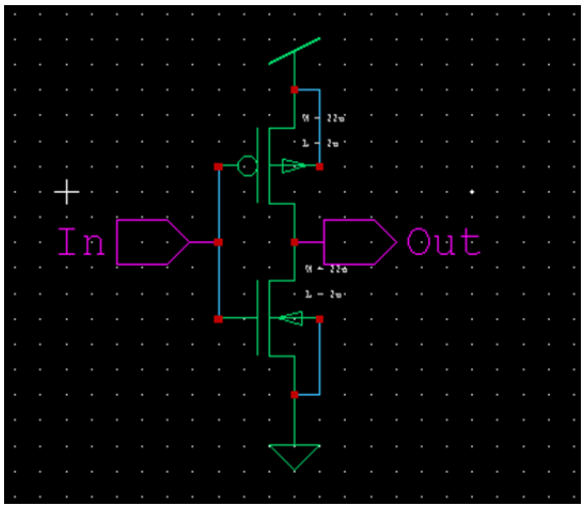

Fig. 1: Schematic of NOT

Layout

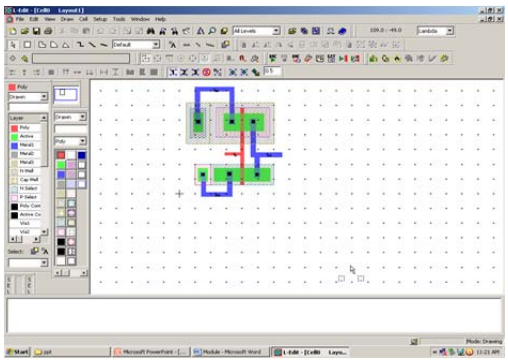

Fig. 2: Layout of NOT

3. WAVEFORMS

i) DC Analysis

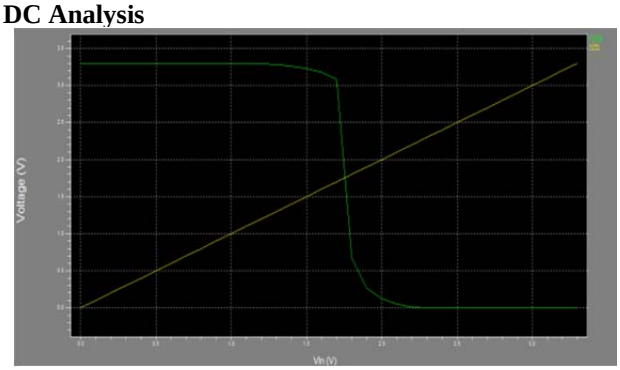

Fig. 3: DC waveform of NOT

ii) AC Analysis

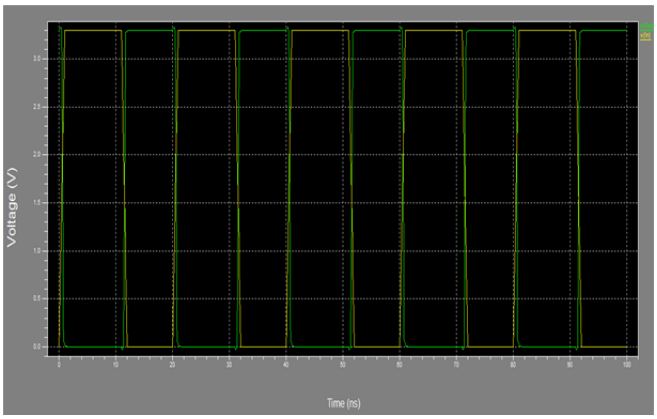

Fig. 4: AC waveform of NOT

B) AND gate

Schematic

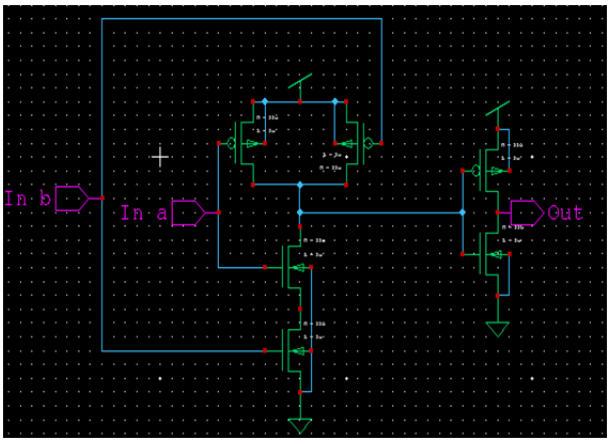

Fig. 5: Schematic of AND

WAVEFORMS

i) DC Analysis

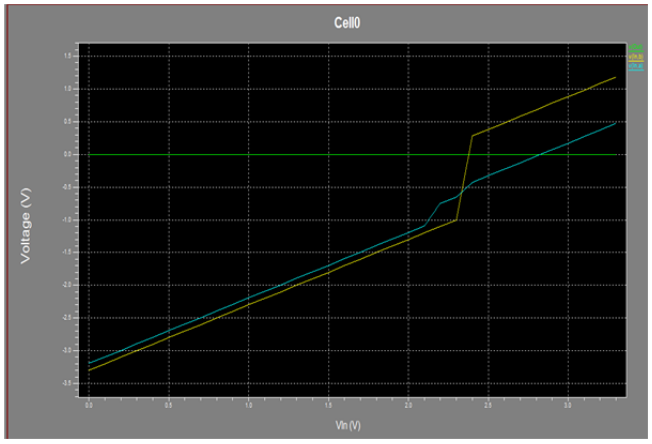

Fig.. 6: DC waveform of AND

ii) AC Analysis

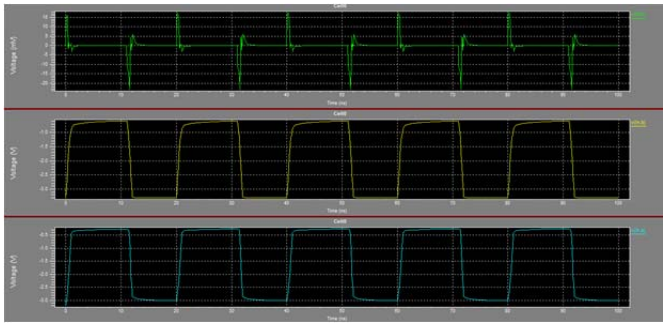

Fig. 7: AC waveform of AND

C) OR gate

Schematic

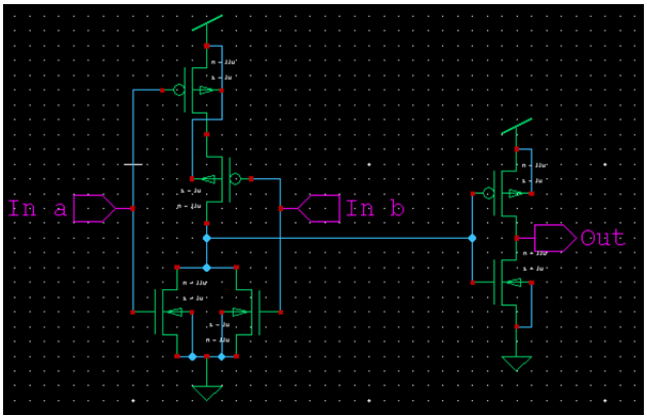

Fig. 8: Schematic of OR

WAVEFORMS

DC Analysis

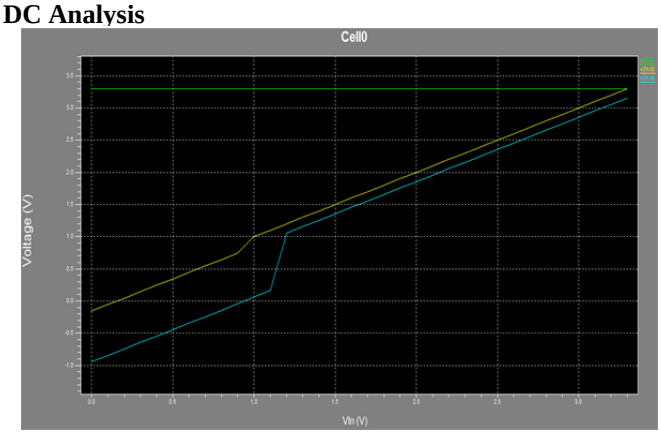

Fig. 9: DC waveform of OR

(ii) AC Analysis

Fig. 10: AC waveform of OR

D) Full Adder

In ALU, full adder forms the core of the entire design. The full adder performs the computing function of the ALU.A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits [4]. It consists of three inputs and two outputs. In our design, we have designated the three inputs as A, B and Cin. The third input Cin represents carry input to the first stage. The outputs are SUM and CARRY. **Figure** shows the logic level diagram of a full adder. The Boolean expressions for the SUM and CARRY bits are as shown below.

SUM = A⊕B ⊕Cin

CARRY = A · B + A· Cin+ B ·C

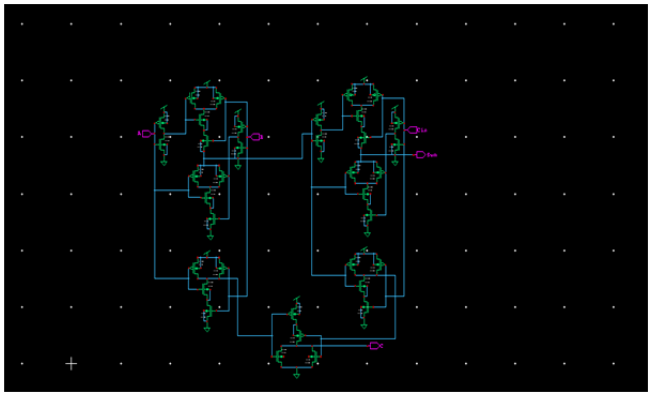

Fig. 11: Schematic of full adder

WAVEFORMS

i)DC Analysis

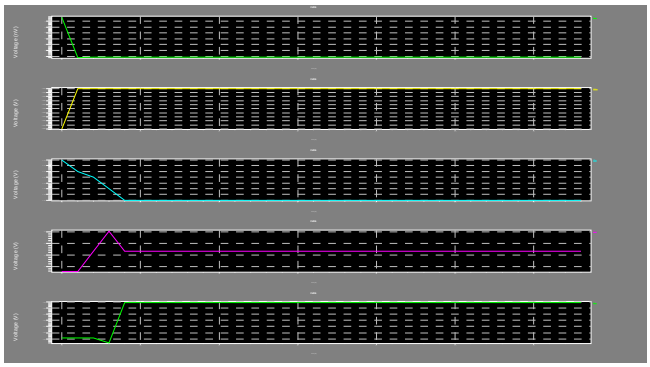

Fig. 12: DC waveform of full adder

ii)AC Analysis

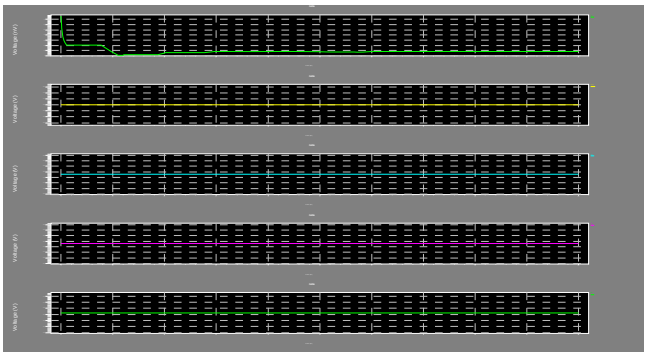

Fig. 13: AC waveform of full adder

E)Full Subtractor

Full Subtractor is a combinational circuit with three inputs A, B and B_{in} and two outputs Difference(D) and Borrow(B_0).

$D = A \oplus B \oplus B_{in}$

$B_0 = A'B_{in} + A'B + BB_{in}$

Schematic

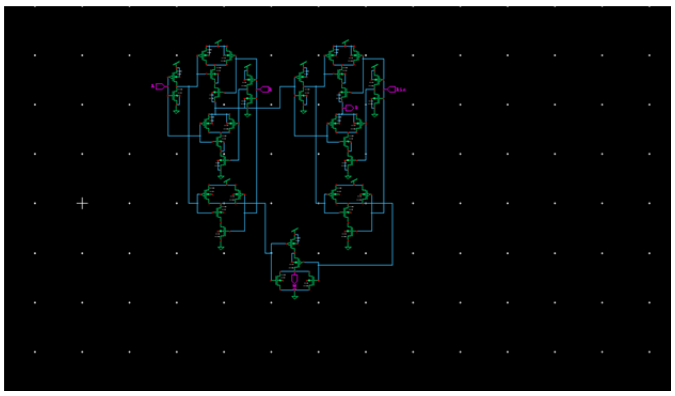

Fig. 14: Schematic of full subtractor

WAVEFORMS

i)DC Analysis

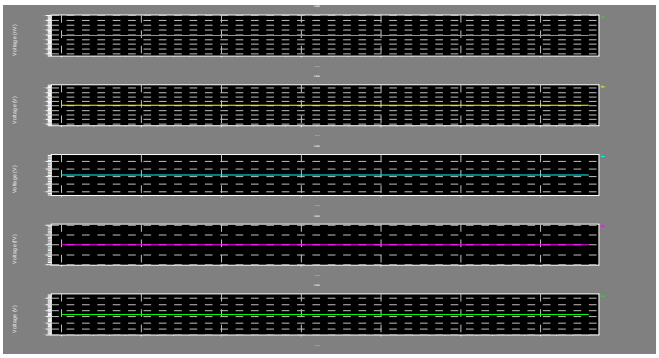

Fig. 15: DC waveform of fullsubtractor

ii)AC Analysis

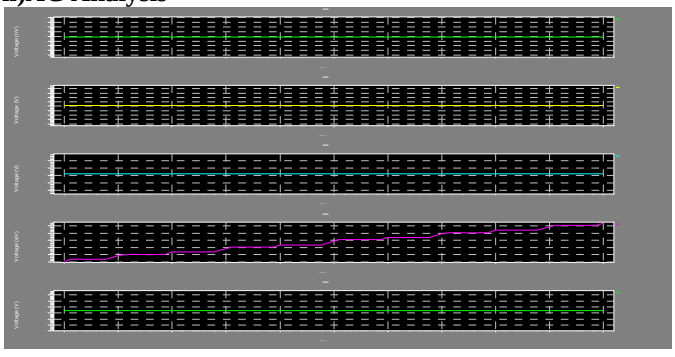

Fig. 16: AC waveform of full subtractor

F)Multiplexer

M**ultiplexer** (or **MUX**) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are

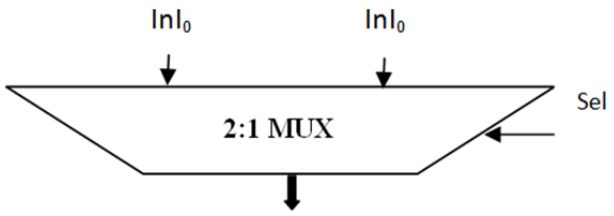

Fig. 17: Block of 2:1 MUX

mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a **data selector**.

Schematic

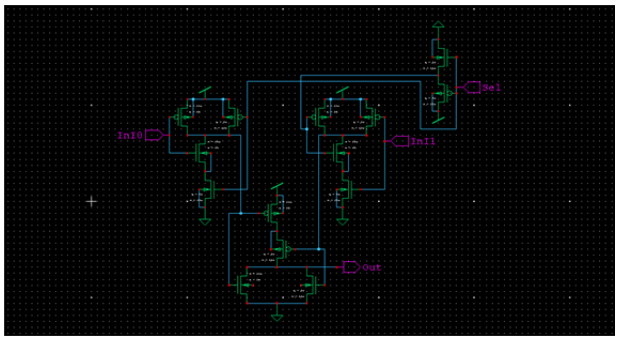

Fig. 18: Schematic of MUX

WAVEFORMS

i)DC Analysis

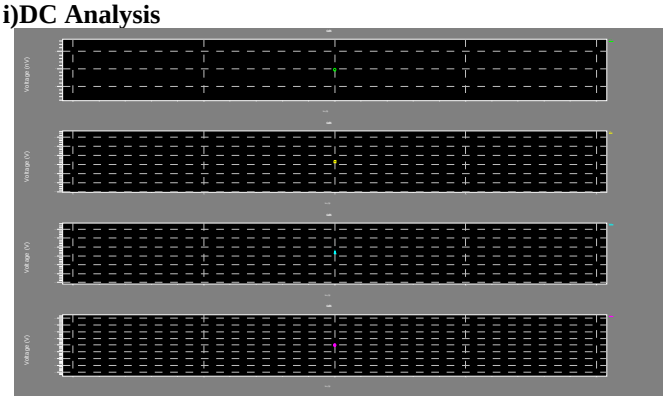

Fig. 19: DC waveform of MUX

ii)AC Analysis

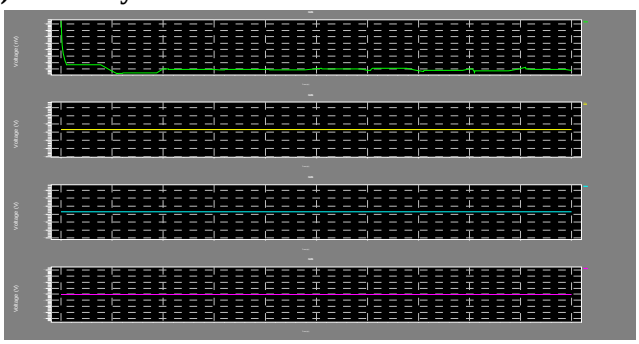

Fig. 20: AC waveform of MUX

V) Arithmetic Logic Unit

A 8-bit ALU has been designed for 3V operation. The ALU can perform various arithmetic and logical operations**.** The basic blocks of a computer are central processing unit (CPU), memory unit, and input/output unit.[5] CPU of the computer is basically the same as the brain of a human being. It contains all the registers, control unit and the arithmetic logic unit (ALU). ALUconsidered as the most important subsystem in a digital computer. An arithmetic logic unit (ALU) is a digital circuit which performs arithmetic, logic and shift operations on two n-bit digital words. Functionally, an ALU can be divided up into three circuits: the arithmetic circuit, the logic circuit and the shift circuit.[6] The 8-bit ALU was formed by combining four Full Adder and four Full Subtractor with five multiplexer as shown in the schematic diagram.

Schematic

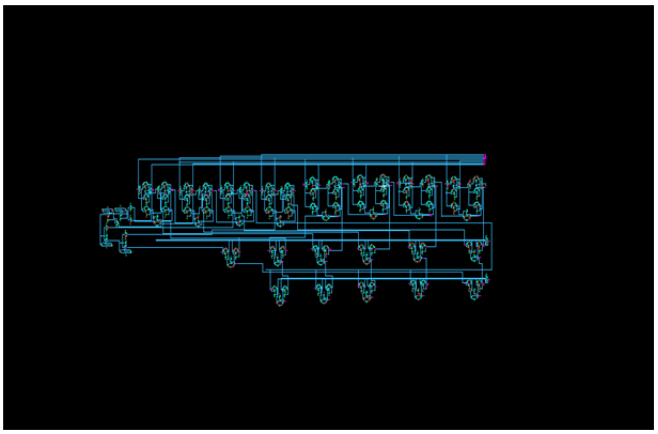

Fig. 21: Schematic of ALU

WAVEFORMS

i)DC Analysis

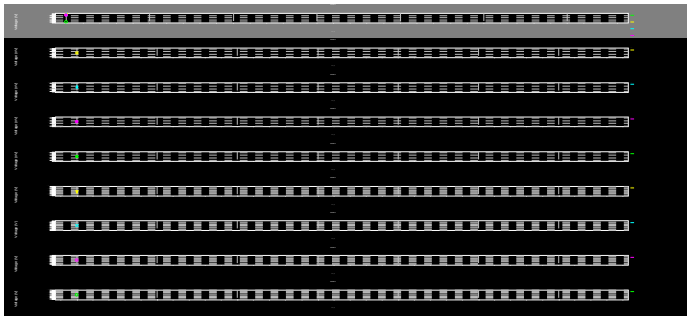

Fig. 22: DC waveform of ALU

ii)AC Analysis

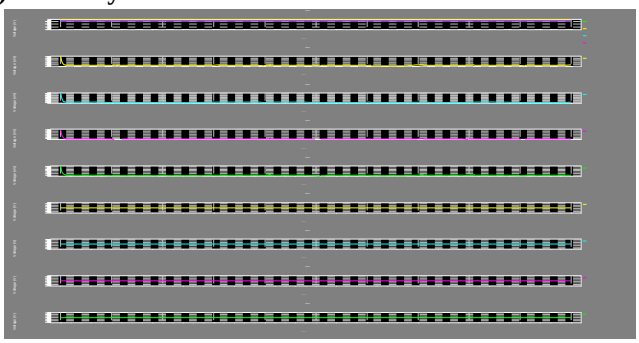

Fig. 23: AC waveform of ALU

4. CONCLUSIONS

Implementation of 8 bit arithmetic logic unit(ALU) is presented . The design was implemented using SPICE code and Tanner tool V12.5. ALU was designed to perform arithmetic operations such as addition and subtraction using 8-bit fast adder, logical operations such as AND, OR, XOR and NOT operations, complement operations and compare. The maximum operating voltage is 3v and power dissipation is 38mW. The ALU was designed for controller used in network interface card.

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